

# LMK02000

## Precision Clock Conditioner with Integrated PLL

### General Description

The LMK02000 precision clock conditioner combines the functions of jitter cleaning/reconditioning, multiplication, and distribution of a reference clock. The device integrates a high performance Integer-N Phase Locked Loop (PLL), three LVDS, and five LVPECL clock output distribution blocks.

Each clock distribution block includes a programmable divider, a phase synchronization circuit, a programmable delay, a clock output mux, and an LVDS or LVPECL output buffer. This allows multiple integer-related and phase-adjusted copies of the reference to be distributed to eight system components.

The clock conditioner comes in a 48-pin LLP package and is footprint compatible with other clocking devices in the same family.

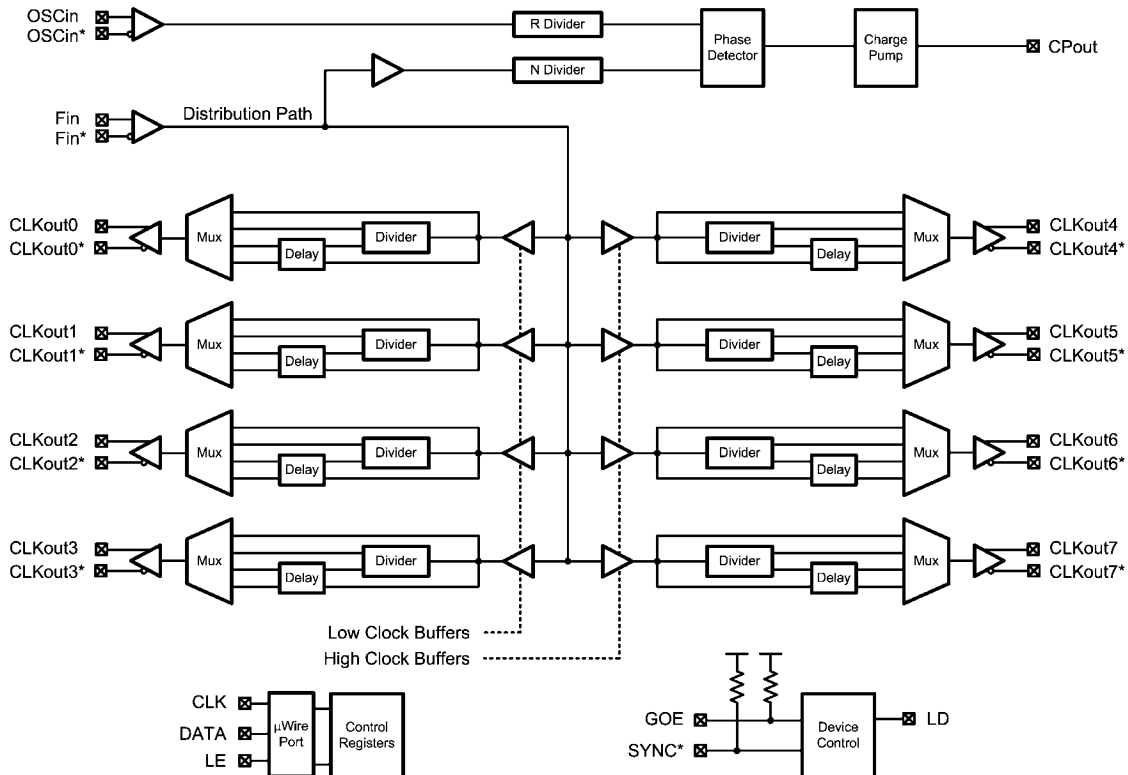
### Features

- 20 fs additive jitter
- Integrated Integer-N PLL with outstanding normalized phase noise contribution of -224 dBc/Hz
- Clock output frequency range of 1 to 800 MHz
- 3 LVDS and 5 LVPECL clock outputs
- Dedicated divider and delay blocks on each clock output
- Pin compatible family of clocking devices
- 3.15 to 3.45 V operation
- Package: 48 pin LLP (7.0 x 7.0 x 0.8 mm)

### Target Applications

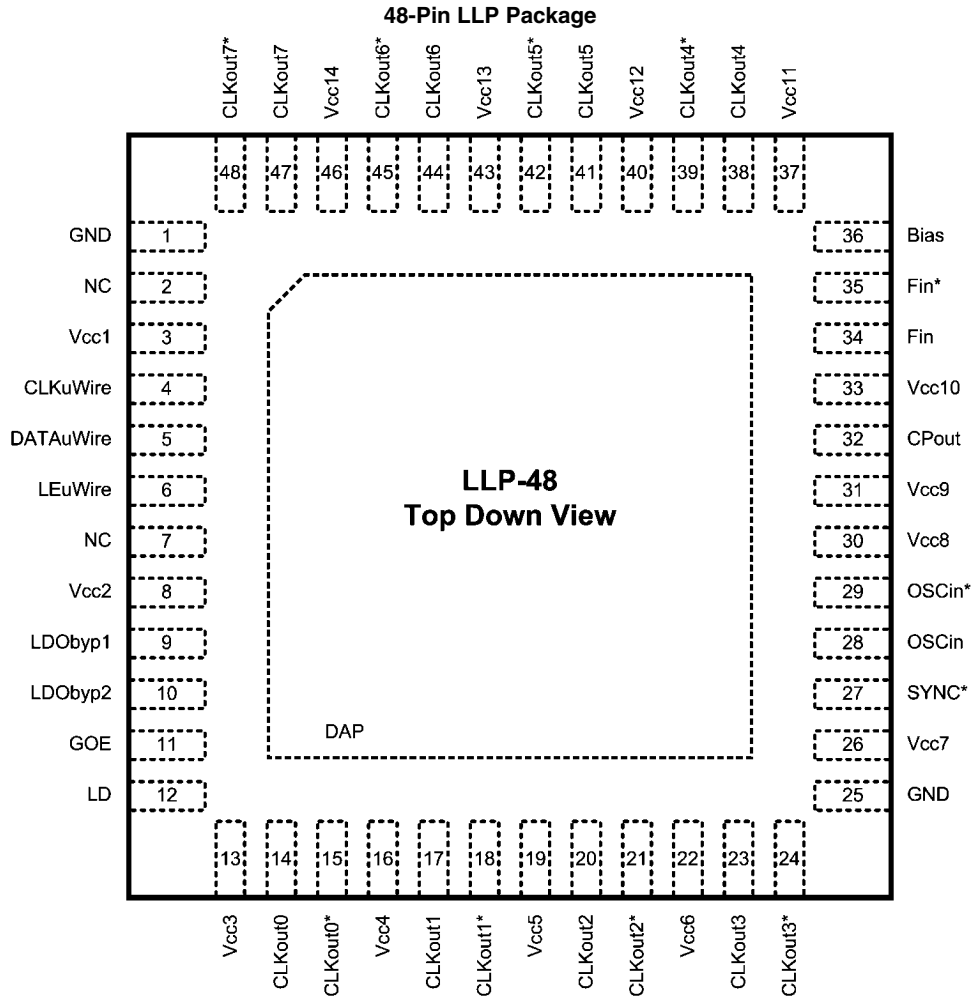
- Data Converter Clocking
- Networking, SONET/SDH, DSLAM
- Wireless Infrastructure
- Medical
- Test and Measurement
- Military / Aerospace

### Functional Block Diagram



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# Connection Diagram



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## Pin Descriptions

| Pin #  | Pin Name  | I/O | Description                                |
|--|---|-----|--|
| 1, 25  | GND   | -   | Ground                                     |
| 2, 7   | NC  | -   | No Connection to these pins                |
| 3, 8, 13, 16, 19, 22, 26, 30, 31, 33, 37, 40, 43, 46 | Vcc1, Vcc2, Vcc3, Vcc4, Vcc5, Vcc6, Vcc7, Vcc8, Vcc9, Vcc10, Vcc11, Vcc12, Vcc13, Vcc14 | -   | Power Supply                               |
| 4  | CLKuWire  | I   | MICROWIRE Clock Input                      |
| 5  | DATAuWire   | I   | MICROWIRE Data Input                       |
| 6  | LEuWire   | I   | MICROWIRE Latch Enable Input               |
| 9, 10  | LDObyp1, LDObyp2  | -   | LDO Bypass                                 |
| 11   | GOE   | I   | Global Output Enable                       |
| 12   | LD  | O   | Lock Detect and Test Output                |
| 14, 15   | CLKout0, CLKout0*   | O   | LVDS Clock Output 0                        |
| 17, 18   | CLKout1, CLKout1*   | O   | LVDS Clock Output 1                        |
| 20, 21   | CLKout2, CLKout2*   | O   | LVDS Clock Output 2                        |
| 23, 24   | CLKout3, CLKout3*   | O   | LVPECL Clock Output 3                      |
| 27   | SYNC*   | I   | Global Clock Output Synchronization        |
| 28, 29   | OSCin, OSCin*   | I   | Oscillator Clock Input; Must be AC coupled |
| 32   | CPout   | O   | Charge Pump Output                         |
| 34, 35   | Fin, Fin*   | I   | Frequency Input; Must be AC coupled        |
| 36   | Bias  | I   | Bias Bypass                                |
| 38, 39   | CLKout4, CLKout4*   | O   | LVPECL Clock Output 4                      |
| 41, 42   | CLKout5, CLKout5*   | O   | LVPECL Clock Output 5                      |
| 44, 45   | CLKout6, CLKout6*   | O   | LVPECL Clock Output 6                      |
| 47, 48   | CLKout7, CLKout7*   | O   | LVPECL Clock Output 7                      |
| DAP  | DAP   | -   | Die Attach Pad is Ground                   |

## Absolute Maximum Ratings (Notes 1, 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

| Parameter                     | Symbol    | Ratings                    | Units |
|-------------------------------|-----------|----------------------------|-------|
| Power Supply Voltage          | $V_{CC}$  | -0.3 to 3.6                | V     |
| Input Voltage                 | $V_{IN}$  | -0.3 to ( $V_{CC} + 0.3$ ) | V     |
| Storage Temperature Range     | $T_{STG}$ | -65 to 150                 | °C    |
| Lead Temperature (solder 4 s) | $T_L$     | +260                       | °C    |
| Junction Temperature          | $T_J$     | 125                        | °C    |

## Recommended Operating Conditions

| Parameter            | Symbol   | Min  | Typ | Max  | Units |
|----------------------|----------|------|-----|------|-------|
| Ambient Temperature  | $T_A$    | -40  | 25  | 85   | °C    |
| Power Supply Voltage | $V_{CC}$ | 3.15 | 3.3 | 3.45 | V     |

**Note 1:** "Absolute Maximum Ratings" indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the Absolute Maximum Ratings or other conditions beyond those indicated in the Recommended Operating Conditions is not implied. The Recommended Operating Conditions indicate conditions at which the device is functional and the device should not be operated beyond such conditions.

**Note 2:** This device is a high performance integrated circuit with ESD handling precautions. Handling of this device should only be done at ESD protected work stations. The device is rated to a HBM-ESD of > 2 kV, a MM-ESD of > 200 V, and a CDM-ESD of > 1.2 kV.

## Package Thermal Resistance

| Package              | $\theta_{JA}$ | $\theta_{J-PAD}$ (Thermal Pad) |
|----------------------|---------------|--------------------------------|
| 48-Lead LLP (Note 3) | 27.4° C/W     | 5.8° C/W                       |

**Note 3:** Specification assumes 16 thermal vias connect the die attach pad to the embedded copper plane on the 4-layer JEDEC board. These vias play a key role in improving the thermal performance of the LLP. It is recommended that the maximum number of vias be used in the board layout.

## Electrical Characteristics (Note 4)

( $3.15\text{ V} \leq V_{CC} \leq 3.45\text{ V}$ ,  $-40\text{ °C} \leq T_A \leq 85\text{ °C}$ , Differential Inputs/Outputs; except as specified. Typical values represent most likely parametric norms at  $V_{CC} = 3.3\text{ V}$ ,  $T_A = 25\text{ °C}$ , and at the Recommended Operation Conditions at the time of product characterization and are not guaranteed).

| Symbol                      | Parameter  | Conditions   | Min | Typ   | Max | Units |
|-----------------------------|--|--|-----|-------|-----|-------|
| <b>Current Consumption</b>  |  |  |     |       |     |       |
| $I_{CC}$                    | Power Supply Current (Note 5)                              | Entire device; CLKout0 & CLKout4 enabled in Bypass Mode      |     | 145.8 |     | mA    |
|                             |  | Entire device; All Outputs Off (no emitter resistors placed) |     | 70    |     |       |
| $I_{CCPD}$                  | Power Down Current   | POWERDOWN = 1  |     | 1     |     | mA    |
| <b>Reference Oscillator</b> |  |  |     |       |     |       |
| $f_{OSCin\ square}$         | Reference Oscillator Input Frequency Range for Square Wave | AC coupled; Differential ( $V_{OD}$ )                        | 1   |       | 200 | MHz   |
| $V_{OSCin\ square}$         | Square Wave Input Voltage for OSCin and OSCin*             |  | 0.2 |       | 1.6 | Vpp   |
| <b>Frequency Input</b>      |  |  |     |       |     |       |
| $f_{Fin}$                   | Frequency Input Frequency Range                            |  | 1   |       | 800 | MHz   |
| $SLEW_{Fin}$                | Frequency Input Slew Rate                                  | (Notes 6, 10)  | 0.5 |       |     | V/ns  |
| $DUTY_{Fin}$                | Frequency Input Duty Cycle                                 |  | 40  |       | 60  | %     |
| $P_{Fin}$                   | Input Power Range for Fin or Fin*                          | AC coupled   | -13 |       | 8   | dBm   |

| Symbol   | Parameter  | Conditions  | Min                                      | Typ     | Max   | Units   |
|--|--|---|--|---------|-------|---------|
| <b>PLL</b>   |  |   |  |         |       |         |
| $f_{COMP}$   | Phase Detector Frequency   |   |  |         | 40    | MHz     |
| $I_{SRCE\_CPout}$  | Charge Pump Source Current   | $V_{CPout} = V_{CC}/2, PLL\_CP\_GAIN = 1x$  |  | 100     |       | $\mu A$ |
|  |  | $V_{CPout} = V_{CC}/2, PLL\_CP\_GAIN = 4x$  |  | 400     |       |         |
|  |  | $V_{CPout} = V_{CC}/2, PLL\_CP\_GAIN = 16x$                                       |  | 1600    |       |         |
|  |  | $V_{CPout} = V_{CC}/2, PLL\_CP\_GAIN = 32x$                                       |  | 3200    |       |         |
| $I_{SINK\_CPout}$  | Charge Pump Sink Current   | $V_{CPout} = V_{CC}/2, PLL\_CP\_GAIN = 1x$  |  | -100    |       | $\mu A$ |
|  |  | $V_{CPout} = V_{CC}/2, PLL\_CP\_GAIN = 4x$  |  | -400    |       |         |
|  |  | $V_{CPout} = V_{CC}/2, PLL\_CP\_GAIN = 16x$                                       |  | -1600   |       |         |
|  |  | $V_{CPout} = V_{CC}/2, PLL\_CP\_GAIN = 32x$                                       |  | -3200   |       |         |
| $I_{CPout\_TRI}$   | Charge Pump TRI-STATE® Current   | $0.5 V < V_{CPout} < V_{CC} - 0.5 V$  |  | 2       | 10    | nA      |
| $I_{CPout\%MIS}$   | Magnitude of Charge Pump Sink vs. Source Current Mismatch                    | $V_{CPout} = V_{CC} / 2$<br>$T_A = 25^\circ C$                                    |  | 3       |       | %       |
| $I_{CPout\_VTUNE}$   | Magnitude of Charge Pump Current vs. Charge Pump Voltage Variation           | $0.5 V < V_{CPout} < V_{CC} - 0.5 V$<br>$T_A = 25^\circ C$                        |  | 4       |       | %       |
| $I_{CPout\_TEMP}$  | Magnitude of Charge Pump Current vs. Temperature Variation                   |   |  | 4       |       | %       |
| PN10kHz  | PLL 1/f Noise at 10 kHz Offset (Note 7) Normalized to 1 GHz Output Frequency | $PLL\_CP\_GAIN = 1x$  |  | -117    |       | dBc/Hz  |
|  |  | $PLL\_CP\_GAIN = 32x$   |  | -122    |       |         |
| PN1Hz  | Normalized Phase Noise Contribution (Note 8)                                 | $PLL\_CP\_GAIN = 1x$  |  | -219    |       | dBc/Hz  |
|  |  | $PLL\_CP\_GAIN = 32x$   |  | -224    |       |         |
| <b>Clock Distribution Section (Note 9) - LVDS Clock Outputs (CLKout0 to CLKout2)</b> |  |   |  |         |       |         |
| $Jitter_{ADD}$   | Additive RMS Jitter (Note 9)   | $R_L = 100 \Omega$<br>Distribution Path = 800 MHz<br>Bandwidth = 12 kHz to 20 MHz | CLKoutX_MUX = Bypass                     |         | 20    | fs      |
|  |  |   | CLKoutX_MUX = Divided<br>CLKoutX_DIV = 4 |         | 75    |         |
| $t_{SKEW}$   | CLKoutX to CLKoutY (Note 10)   | Equal loading and identical clock configuration<br>$R_L = 100 \Omega$             | -30                                      | $\pm 4$ | 30    | ps      |
| $V_{OD}$   | Differential Output Voltage  | $R_L = 100 \Omega$  | 250                                      | 350     | 450   | mV      |
| $\Delta V_{OD}$  | Change in magnitude of $V_{OD}$ for complementary output states              | $R_L = 100 \Omega$  | -50                                      |         | 50    | mV      |
| $V_{OS}$   | Output Offset Voltage  | $R_L = 100 \Omega$  | 1.070                                    | 1.25    | 1.370 | V       |
| $\Delta V_{OS}$  | Change in magnitude of $V_{OS}$ for complementary output states              | $R_L = 100 \Omega$  | -35                                      |         | 35    | mV      |
| $I_{SA}$<br>$I_{SB}$   | Clock Output Short Circuit Current single ended                              | Single ended outputs shorted to GND   | -24                                      |         | 24    | mA      |
| $I_{SAB}$  | Clock Output Short Circuit Current differential                              | Complementary outputs tied together   | -12                                      |         | 12    | mA      |

| Symbol   | Parameter                    | Conditions  | Min  | Typ           | Max | Units |
|--|------------------------------|---|--|---------------|-----|-------|
| <b>Clock Distribution Section (Note 9) - LVPECL Clock Outputs (CLKout3 to CLKout7)</b> |                              |   |  |               |     |       |
| Jitter <sub>ADD</sub>  | Additive RMS Jitter (Note 9) | R <sub>L</sub> = 100 Ω<br>Distribution Path =<br>800 MHz<br>Bandwidth =<br>12 kHz to 20 MHz | CLKoutX_MUX<br>= Bypass                        |               | 20  | fs    |
|  |                              |   | CLKoutX_MUX<br>= Divided<br>CLKoutX_DIV =<br>4 |               | 75  |       |
| t <sub>SKEW</sub>  | CLKoutX to CLKoutY (Note 10) | Equal loading and identical clock<br>configuration<br>Termination = 50 Ω to Vcc - 2 V       | -30  | ±3            | 30  | ps    |
| V <sub>OH</sub>  | Output High Voltage          | Termination = 50 Ω to Vcc - 2 V   |  | Vcc -<br>0.98 |     | V     |
| V <sub>OL</sub>  | Output Low Voltage           |   |  | Vcc -<br>1.8  |     | V     |
| V <sub>OD</sub>  | Differential Output Voltage  |   | 660  | 810           | 965 | mV    |
| <b>Digital LVTTTL Interfaces (Note 11)</b>   |                              |   |  |               |     |       |
| V <sub>IH</sub>  | High-Level Input Voltage     |   | 2.0  |               | Vcc | V     |
| V <sub>IL</sub>  | Low-Level Input Voltage      |   |  |               | 0.8 | V     |
| I <sub>IH</sub>  | High-Level Input Current     | V <sub>IH</sub> = Vcc   | -5.0   |               | 5.0 | µA    |
| I <sub>IL</sub>  | Low-Level Input Current      | V <sub>IL</sub> = 0   | -40.0  |               | 5.0 | µA    |
| V <sub>OH</sub>  | High-Level Output Voltage    | I <sub>OH</sub> = +500 µA   |  | Vcc -<br>0.4  |     | V     |
| V <sub>OL</sub>  | Low-Level Output Voltage     | I <sub>OL</sub> = -500 µA   |  |               | 0.4 | V     |
| <b>Digital MICROWIRE Interfaces (Note 12)</b>  |                              |   |  |               |     |       |
| V <sub>IH</sub>  | High-Level Input Voltage     |   | 1.6  |               | Vcc | V     |
| V <sub>IL</sub>  | Low-Level Input Voltage      |   |  |               | 0.4 | V     |
| I <sub>IH</sub>  | High-Level Input Current     | V <sub>IH</sub> = Vcc   | -5.0   |               | 5.0 | µA    |
| I <sub>IL</sub>  | Low-Level Input Current      | V <sub>IL</sub> = 0   | -5.0   |               | 5.0 | µA    |
| <b>MICROWIRE Timing</b>  |                              |   |  |               |     |       |
| t <sub>CS</sub>  | Data to Clock Set Up Time    | See Data Input Timing   | 25   |               |     | ns    |
| t <sub>CH</sub>  | Data to Clock Hold Time      | See Data Input Timing   | 8  |               |     | ns    |
| t <sub>CWH</sub>   | Clock Pulse Width High       | See Data Input Timing   | 25   |               |     | ns    |
| t <sub>CWL</sub>   | Clock Pulse Width Low        | See Data Input Timing   | 25   |               |     | ns    |
| t <sub>ES</sub>  | Clock to Enable Set Up Time  | See Data Input Timing   | 25   |               |     | ns    |
| t <sub>CES</sub>   | Enable to Clock Set Up Time  | See Data Input Timing   | 25   |               |     | ns    |
| t <sub>EWH</sub>   | Enable Pulse Width High      | See Data Input Timing   | 25   |               |     | ns    |

**Note 4:** The Electrical Characteristics tables list guaranteed specifications under the listed Recommended Operating Conditions except as otherwise modified or specified by the Electrical Characteristics Conditions and/or Notes. Typical specifications are estimations only and are not guaranteed.

**Note 5:** See 3.4 for more current consumption / power dissipation calculation information.

**Note 6:** For all frequencies the slew rate, SLEW<sub>F<sub>in</sub></sub>, is measured between 20% and 80%.

**Note 7:** A specification in modeling PLL in-band phase noise is the 1/f flicker noise, L<sub>PLL\_flicker</sub>(f), which is dominant close to the carrier. Flicker noise has a 10 dB/decade slope. PN10kHz is normalized to a 10 kHz offset and a 1 GHz carrier frequency. PN10kHz = L<sub>PLL\_flicker</sub>(10 kHz) - 20log(Fout / 1 GHz), where L<sub>PLL\_flicker</sub>(f) is the single side band phase noise of only the flicker noise's contribution to total noise, L(f). To measure L<sub>PLL\_flicker</sub>(f) it is important to be on the 10 dB/decade slope close to the carrier. A high phase detector frequency and a clean crystal are important to isolating this noise source from the total phase noise, L(f). L<sub>PLL\_flicker</sub>(f) can be masked by the reference oscillator performance if a low power or noisy source is used. The total PLL inband phase noise performance is the sum of L<sub>PLL\_flicker</sub>(f) and L<sub>PLL\_flat</sub>(f).

**Note 8:** A specification in modeling PLL in-band phase noise is the Normalized Phase Noise Contribution, L<sub>PLL\_flat</sub>(f), of the PLL and is defined as PN1Hz = L<sub>PLL\_flat</sub>(f) - 20log(N) - 10log(f<sub>COMP</sub>). L<sub>PLL\_flat</sub>(f) is the single side band phase noise measured at an offset frequency, f, in a 1 Hz Bandwidth and f<sub>COMP</sub> is the phase detector frequency of the synthesizer. L<sub>PLL\_flat</sub>(f) contributes to the total noise, L(f). To measure L<sub>PLL\_flat</sub>(f) the offset frequency, f, must be chosen sufficiently smaller than the loop bandwidth of the PLL, and yet large enough to avoid a substantial noise contribution from the reference and flicker noise. L<sub>PLL\_flat</sub>(f) can be masked by the reference oscillator performance if a low power or noisy source is used.

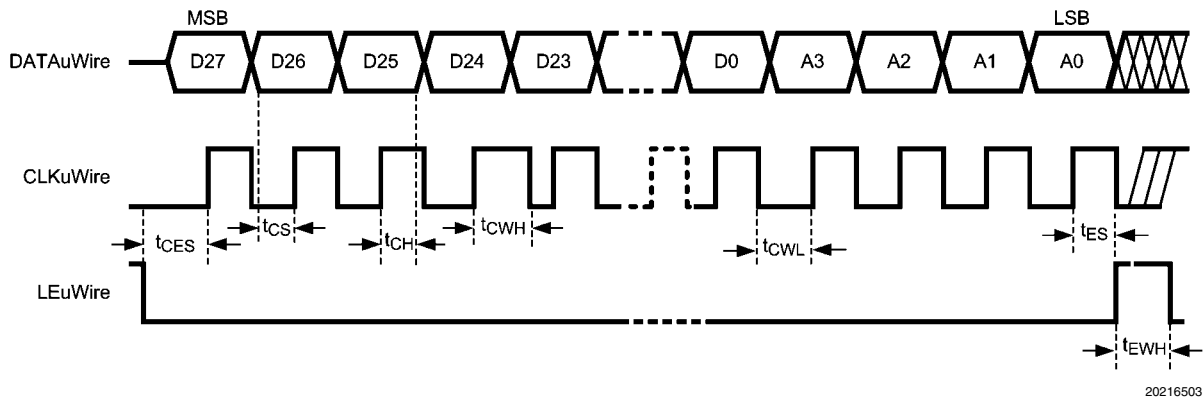
**Note 9:** The Clock Distribution Section includes all parts of the device except the PLL section. Typical Additive Jitter specifications apply to the clock distribution section only.

**Note 10:** Specification is guaranteed by characterization and is not tested in production.

**Note 11:** Applies to GOE, LD, and SYNC\*.

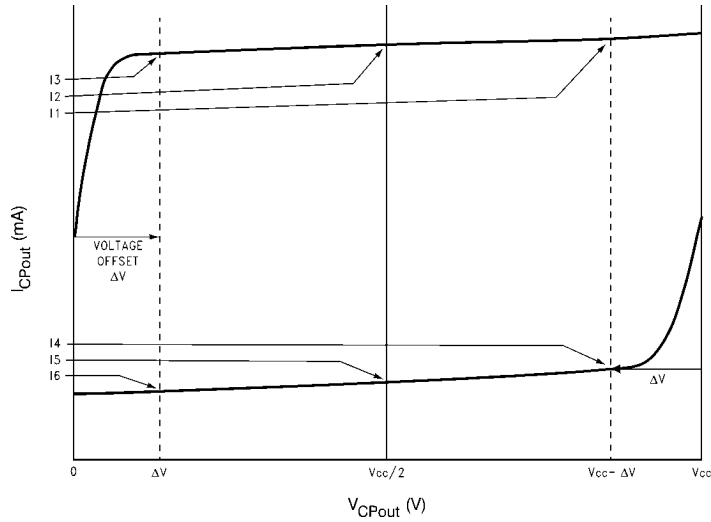
**Note 12:** Applies to CLKuWire, DATAuWire, and LEuWire.

## Serial Data Timing Diagram



Data bits set on the DATAuWire signal are clocked into a shift register, MSB first, on each rising edge of the CLKuWire signal. On the rising edge of the LEuWire signal, the data is sent from the shift register to the addressed register determined by the LSB bits. After the programming is complete the CLKuWire, DATAuWire, and LEuWire signals should be returned to a low state.

# Charge Pump Current Specification Definitions



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I1 = Charge Pump Sink Current at  $V_{CPout} = V_{cc} - \Delta V$

I2 = Charge Pump Sink Current at  $V_{CPout} = V_{cc}/2$

I3 = Charge Pump Sink Current at  $V_{CPout} = \Delta V$

I4 = Charge Pump Source Current at  $V_{CPout} = V_{cc} - \Delta V$

I5 = Charge Pump Source Current at  $V_{CPout} = V_{cc}/2$

I6 = Charge Pump Source Current at  $V_{CPout} = \Delta V$

$\Delta V$  = Voltage offset from the positive and negative supply rails. Defined to be 0.5 V for this device.

## Charge Pump Output Current Magnitude Variation vs. Charge Pump Output Voltage

$$I_{CPout} \text{ Vs } V_{CPout} = \frac{|I1| - |I3|}{|I1| + |I3|} \times 100\%$$

$$= \frac{|I4| - |I6|}{|I4| + |I6|} \times 100\%$$

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## Charge Pump Sink Current vs. Charge Pump Output Source Current Mismatch

$$I_{CPout} \text{ Sink Vs } I_{CPout} \text{ Source} = \frac{|I2| - |I5|}{|I2| + |I5|} \times 100\%$$

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## Charge Pump Output Current Magnitude Variation vs. Temperature

$$I_{CPout} \text{ Vs } T_A = \frac{|I2|_{T_A} - |I2|_{T_A=25^\circ C}}{|I2|_{T_A=25^\circ C}} \times 100\%$$

$$= \frac{|I5|_{T_A} - |I5|_{T_A=25^\circ C}}{|I5|_{T_A=25^\circ C}} \times 100\%$$

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# 1.0 Functional Description

The LMK02000 precision clock conditioner combines the functions of jitter cleaning/reconditioning, multiplication, and distribution of a reference clock. The device integrates a high performance Integer-N Phase Locked Loop (PLL), three LVDS, and five LVPECL clock output distribution blocks.

Each clock distribution block includes a programmable divider, a phase synchronization circuit, a programmable delay, a clock output mux, and an LVDS or LVPECL output buffer. This allows multiple integer-related and phase-adjusted copies of the reference to be distributed to eight system components.

The clock conditioner comes in a 48-pin LLP package and is footprint compatible with other clocking devices in the same family.

## 1.1 BIAS PIN

To properly use the device, bypass Bias (pin 36) with a low leakage 1  $\mu$ F capacitor connected to Vcc. This is important for low noise performance.

## 1.2 LDO BYPASS

To properly use the device, bypass LDObyp1 (pin 9) with a 10  $\mu$ F capacitor and LDObyp2 (pin 10) with a 0.1  $\mu$ F capacitor.

## 1.3 OSCILLATOR INPUT PORT (OSCin, OSCin\*)

The purpose of OSCin is to provide the PLL with a reference signal. The OSCin port must be AC coupled, refer to the System Level Diagram in the Application Information section. The OSCin port may be driven single endedly by AC grounding OSCin\* with a 0.1  $\mu$ F capacitor.

## 1.4 FREQUENCY INPUT PORT (Fin, Fin\*)

The purpose of Fin is to provide the PLL with a feedback signal from an external oscillator. The Fin port may be driven single endedly by AC grounding Fin\*.

## 1.5 CLKout DELAYS

Each individual clock output includes a delay adjustment. Clock output delay registers (CLKoutX\_DLY) support a 150 ps step size and range from 0 to 2250 ps of total delay.

## 1.6 LVDS/LVPECL OUTPUTS

Each LVDS or LVPECL output may be disabled individually by programming the CLKoutX\_EN bits. All the outputs may be disabled simultaneously by pulling the GOE pin low or programming EN\_CLKout\_Global to 0.

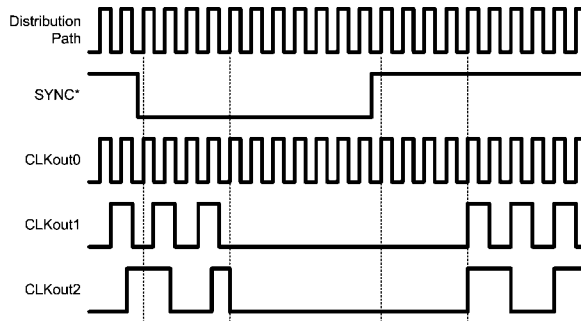
## 1.7 GLOBAL CLOCK OUTPUT SYNCHRONIZATION

The SYNC\* pin synchronizes the clock outputs. When the SYNC\* pin is held in a logic low state, the divided outputs are also held in a logic low state. When the SYNC\* pin goes high, the divided clock outputs are activated and will transition to a high state simultaneously. Clocks in the bypassed state are not affected by SYNC\* and are always synchronized with the divided outputs.

The SYNC\* pin must be held low for greater than one clock cycle of the Frequency Input port, also known as the distribution path. Once this low event has been registered, the outputs will not reflect the low state for four more cycles. Similarly once the SYNC\* pin becomes high, the outputs will not simultaneously transition high until four more distribution path clock cycles have passed. See the timing diagram below for further detail. In the timing diagram below the clocks are pro-

grammed as CLKout0\_MUX = Bypassed, CLKout1\_MUX = Divided, CLKout1\_DIV = 2, CLKout2\_MUX = Divided, and CLKout2\_DIV = 4.

## SYNC\* Timing Diagram



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The SYNC\* pin provides an internal pull-up resistor as shown on the functional block diagram. If the SYNC\* pin is not terminated externally the clock outputs will operate normally. If the SYNC\* function is not used, clock output synchronization is not guaranteed.

## 1.8 CLKout OUTPUT STATES

Each clock output may be individually enabled with the CLKoutX\_EN bits. Each individual output enable control bit is gated with the Global Output Enable input pin (GOE) and the Global Output Enable bit (EN\_CLKout\_Global).

All clock outputs can be disabled simultaneously if the GOE pin is pulled low by an external signal or EN\_CLKout\_Global is set to 0.

| CLKoutX_EN bit | EN_CLKout_Global bit | GOE pin           | Clock X Output State |
|----------------|----------------------|-------------------|----------------------|
| 1              | 1                    | Low               | Low                  |
| Don't care     | 0                    | Don't care        | Off                  |
| 0              | Don't care           | Don't care        | Off                  |
| 1              | 1                    | High / No Connect | Enabled              |

When an LVDS output is in the Off state, the outputs are at a voltage of approximately 1.5 volts. When an LVPECL output is in the Off state, the outputs are at a voltage of approximately 1 volt.

## 1.9 GLOBAL OUTPUT ENABLE AND LOCK DETECT

The GOE pin provides an internal pull-up resistor. If it is not terminated externally, the clock output states are determined by the Clock Output Enable bits (CLKoutX\_EN) and the EN\_CLKout\_Global bit.

By programming the PLL\_MUX register to Digital Lock Detect Active High (See 2.5.2), the Lock Detect (LD) pin can be connected to the GOE pin in which case all outputs are set low automatically if the synthesizer is not locked.

## 1.10 POWER ON RESET

When supply voltage to the device increases monotonically from ground to Vcc, the power on reset circuit sets all registers to their default values, see 2.3.1 for more information on default register values. Voltage should be applied to all Vcc pins simultaneously.

## 2.0 General Programming Information

The LMK02000 device is programmed using several 32-bit registers which control the device's operation. The registers consist of a data field and an address field. The last 4 register bits, ADDR[3:0] form the address field. The remaining 28 bits form the data field DATA[27:0].

During programming, LEuWire is low and serial data is clocked in on the rising edge of clock (MSB first). When LEuWire goes high, data is transferred to the register bank selected by the address field. Only registers R0 to R7, R11, R14, and R15 need to be programmed for proper device operation.

It is required to program register R14.

### 2.1 RECOMMENDED PROGRAMMING SEQUENCE

The recommended programming sequence involves programming R0 with the reset bit set (RESET = 1) to ensure the device is in a default state. It is not necessary to program R0 again, but if R0 is programmed again, the reset bit is programmed clear (RESET = 0). Registers are programmed in order with R15 being the last register programmed. An example programming sequence is shown below.

- Program R0 with the reset bit set (RESET = 1). This ensures the device is in a default state. When the reset bit is set in R0, the other R0 bits are ignored.
  - If R0 is programmed again, the reset bit is programmed clear (RESET = 0).
- Program R0 to R7 as necessary with desired clocks with appropriate enable, mux, divider, and delay settings.
- Program R11 with DIV4 setting if necessary.
- Program R14 with global clock output bit, power down setting, PLL mux setting, and PLL R divider. It is required to program register R14.
  - R14 must be programmed in accordance with the register map as shown in the register map (see 2.2).
- Program R15 with PLL charge pump gain, and PLL N divider.

## 2.2 LMK02000 REGISTER MAP

| Register | 31          | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17                | 16                | 15                | 14                | 13                | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----------|-------------|----|----|----|----|----|----|----|----|----|----|----|----|----|-------------------|-------------------|-------------------|-------------------|-------------------|----|----|----|---|---|---|---|---|---|---|---|---|---|
|          | Data [27:0] |    |    |    |    |    |    |    |    |    |    |    |    |    |                   |                   | A3                | A2                | A1                | A0 |    |    |   |   |   |   |   |   |   |   |   |   |
| R0       | RESET       | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0                 | CLKout0_MUX [1:0] | CLKout0_EN        | CLKout0_DIV [7:0] | CLKout0_DLY [3:0] |    |    |    |   |   |   |   |   |   |   |   |   |   |
| R1       | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | CLKout1_MUX [1:0] | CLKout1_EN        | CLKout1_DIV [7:0] | CLKout1_DLY [3:0] |                   |    |    |    |   |   |   |   |   |   |   |   |   |   |
| R2       | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | CLKout2_MUX [1:0] | CLKout2_EN        | CLKout2_DIV [7:0] | CLKout2_DLY [3:0] |                   |    |    |    |   |   |   |   |   |   |   |   |   |   |
| R3       | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | CLKout3_MUX [1:0] | CLKout3_EN        | CLKout3_DIV [7:0] | CLKout3_DLY [3:0] |                   |    |    |    |   |   |   |   |   |   |   |   |   |   |
| R4       | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | CLKout4_MUX [1:0] | CLKout4_EN        | CLKout4_DIV [7:0] | CLKout4_DLY [3:0] |                   |    |    |    |   |   |   |   |   |   |   |   |   |   |
| R5       | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | CLKout5_MUX [1:0] | CLKout5_EN        | CLKout5_DIV [7:0] | CLKout5_DLY [3:0] |                   |    |    |    |   |   |   |   |   |   |   |   |   |   |
| R6       | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | CLKout6_MUX [1:0] | CLKout6_EN        | CLKout6_DIV [7:0] | CLKout6_DLY [3:0] |                   |    |    |    |   |   |   |   |   |   |   |   |   |   |
| R7       | 0           | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | CLKout7_MUX [1:0] | CLKout7_EN        | CLKout7_DIV [7:0] | CLKout7_DLY [3:0] |                   |    |    |    |   |   |   |   |   |   |   |   |   |   |

| Register | 31                   | 30 | 29 | 28 | 27               | 26        | 25              | 24         | 23               | 22 | 21 | 20              | 19 | 18 | 17 | 16 | 15   | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |   |   |   |
|----------|----------------------|----|----|----|------------------|-----------|-----------------|------------|------------------|----|----|-----------------|----|----|----|----|------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| R11      | 0                    | 0  | 0  | 0  | 0                | 0         | 0               | 0          | 1                | 0  | 0  | 0               | 0  | 0  | 1  | 0  | DIV4 | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 |   |   |   |   |   |   |
| R14      | 0                    | 0  | 1  | 0  | EN_CLKout_Global | POWERDOWN | TRI-STATE       | PLL_CP_POL | PLL_MUX<br>[3:0] |    |    | PLL_R<br>[11:0] |    |    |    |    |      |    |    |    |    |    | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R15      | PLL_CP_GAIN<br>[1:0] |    |    | 0  | 0                | 0         | PLL_N<br>[17:0] |            |                  |    |    |                 |    |    |    |    |      | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |   |   |

### 2.3 REGISTER R0 to R7

Registers R0 through R7 control the eight clock outputs. Register R0 controls CLKout0, Register R1 controls CLKout1, and so on. There is one additional bit in register R0 called RESET. Aside from this, the functions of these bits are identical. The X in CLKoutX\_MUX, CLKoutX\_DIV, CLKoutX\_DLY, and CLKoutX\_EN denote the actual clock output which may be from 0 to 7.

### 2.3.1 RESET Bit -- R0 only

This bit is only in register R0. The use of this bit is optional and it should be set to '0' if not used. Setting this bit to a '1' forces all registers to their power on reset condition and therefore automatically clears this bit. If this bit is set, all other R0 bits are ignored and R0 needs to be programmed again if used with its proper values and RESET = 0.

| Bit Name         | Default Bit Value | Bit State                  | Bit Description                | Register | Bit Location |
|------------------|-------------------|----------------------------|--------------------------------|----------|--------------|
| RESET            | 0                 | No reset, normal operation | Reset to power on defaults     | R0       | 31           |
| CLKoutX_MUX      | 0                 | Bypassed                   | CLKoutX mux mode               | R0 to R7 | 18:17        |
| CLKoutX_EN       | 0                 | Disabled                   | CLKoutX enable                 |          | 16           |
| CLKoutX_DIV      | 1                 | Divide by 2                | CLKoutX clock divide           |          | 15:8         |
| CLKoutX_DLY      | 0                 | 0 ps                       | CLKoutX clock delay            |          | 7:4          |
| DIV4             | 0                 | PDF ≤ 20 MHz               | Phase Detector Frequency       |          | R11          |
| EN_CLKout_Global | 1                 | Normal - CLKouts normal    | Global clock output enable     | R14      | 27           |
| POWERDOWN        | 0                 | Normal - Device active     | Device power down              |          | 26           |
| PLL_CP_TRI       | 0                 | Normal - PLL active        | TRI-STATE PLL charge pump      |          | 25           |
| PLL_CP_POL       | 0                 | Negative Polarity CP       | Polarity of charge pump        |          | 24           |
| PLL_MUX          | 0                 | Disabled                   | Multiplexer control for LD pin |          | 23:20        |
| PLL_R            | 10                | R divider = 10             | PLL R divide value             |          | 19:8         |
| PLL_CP_GAIN      | 0                 | 100 uA                     | Charge pump current            | R15      | 31:30        |
| PLL_N            | 760               | N divider = 760            | PLL N divide value             |          | 25:8         |

### 2.3.2 CLKoutX\_MUX[1:0] -- Clock Output Multiplexers

These bits control the Clock Output Multiplexer for each clock output. Changing between the different modes changes the blocks in the signal path and therefore incurs a delay relative to the bypass mode. The different MUX modes and associated delays are listed below.

| CLKoutX_MUX [1:0] | Mode                | Added Delay Relative to Bypass Mode             |
|-------------------|---------------------|---|
| 0                 | Bypassed (default)  | 0 ps  |
| 1                 | Divided             | 100 ps  |
| 2                 | Delayed             | 400 ps<br>(In addition to the programmed delay) |
| 3                 | Divided and Delayed | 500 ps<br>(In addition to the programmed delay) |

### 2.3.3 CLKoutX\_DIV[7:0] -- Clock Output Dividers

These bits control the clock output divider value. In order for these dividers to be active, the respective CLKoutX\_MUX (See 2.3.2) bit must be set to either "Divided" or "Divided and Delayed" mode. After all the dividers are programmed, the SYNC\* pin must be used to ensure that all edges of the clock outputs are aligned (See 1.7). By adding the divider block to the output path a fixed delay of approximately 100 ps is incurred.

The actual Clock Output Divide value is twice the binary value programmed as listed in the table below.

| CLKoutX_DIV[7:0] |   |   |   |   |   |   |   | Clock Output Divider value |
|------------------|---|---|---|---|---|---|---|----------------------------|
| 0                | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Invalid                    |
| 0                | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 2 (default)                |
| 0                | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 4                          |
| 0                | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 6                          |
| 0                | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 8                          |
| 0                | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 10                         |
| .                | . | . | . | . | . | . | . | ...                        |
| 1                | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 510                        |

### 2.3.4 CLKoutX\_DLY[3:0] -- Clock Output Delays

These bits control the delay stages for each clock output. In order for these delays to be active, the respective CLKoutX\_MUX (See 2.3.2) bit must be set to either "Delayed" or "Divided and Delayed" mode. By adding the delay block to the output path a fixed delay of approximately 400 ps is incurred in addition to the delay shown in the table below.

| CLKoutX_DLY[3:0] | Delay (ps)  |
|------------------|-------------|
| 0                | 0 (default) |
| 1                | 150         |
| 2                | 300         |
| 3                | 450         |
| 4                | 600         |
| 5                | 750         |
| 6                | 900         |
| 7                | 1050        |
| 8                | 1200        |
| 9                | 1350        |
| 10               | 1500        |
| 11               | 1650        |
| 12               | 1800        |
| 13               | 1950        |

| CLKoutX_DLY[3:0] | Delay (ps) |
|------------------|------------|
| 14               | 2100       |
| 15               | 2250       |

### 2.3.5 CLKoutX\_EN bit -- Clock Output Enables

These bits control whether an individual clock output is enabled or not. If the EN\_CLKout\_Global bit (See 2.5.4) is set to zero or if GOE pin is held low, all CLKoutX\_EN bit states will be ignored and all clock outputs will be disabled. See 1.8 for more information on CLKout states.

| CLKoutX_EN bit | Conditions                    | CLKoutX State      |
|----------------|-------------------------------|--------------------|
| 0              | EN_CLKout_Global bit = 1      | Disabled (default) |
| 1              | GOE pin = High / No Connect 1 | Enabled            |

### 2.4 REGISTER R11

This register only has one bit and only needs to be programmed in the case that the phase detector frequency is greater than 20 MHz and digital lock detect is used. Otherwise, it is automatically defaulted to the correct values.

#### 2.4.1 DIV4

This bit divides the frequency presented to the digital lock detect circuitry by 4. It is necessary to get a reliable output from the digital lock detect output in the case of a phase detector frequency greater than 20 MHz.

| DIV4 | Digital Lock Detect Circuitry Mode                            |
|------|---|
| 0    | Not divided; Phase detector frequency $\leq$ 20 MHz (default) |
| 1    | Divided by 4; Phase detector frequency > 20 MHz               |

### 2.5 REGISTER R14

The LMK02000 requires register R14 to be programmed as shown in the register map (see 2.2).

#### 2.5.1 PLL\_R[11:0] -- R Divider Value

These bits program the PLL R Divider and are programmed in binary fashion.

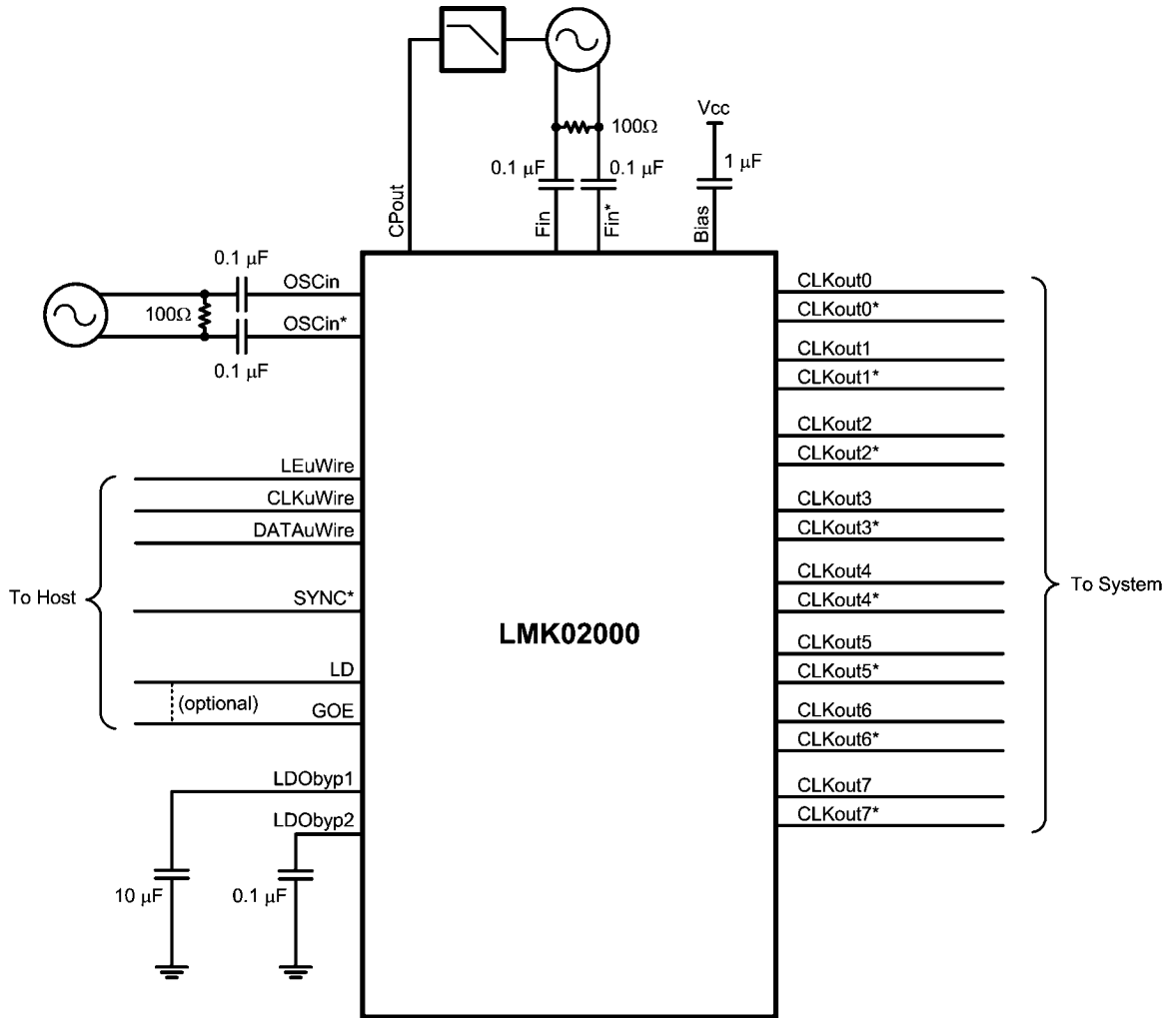
| PLL_R[11:0] |   |   |   |   |   |   |   |   |   |   | PLL R Divide Value |
|-------------|---|---|---|---|---|---|---|---|---|---|--------------------|
| 0           | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Invalid            |
| 0           | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1                  |
| 0           | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 2                  |
| .           | . | . | . | . | . | . | . | . | . | . | ...                |
| 0           | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 10 (default)       |
| .           | . | . | . | . | . | . | . | . | . | . | ...                |
| 1           | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 4095               |



### 3.0 Application Information

#### 3.1 SYSTEM LEVEL DIAGRAM

The following shows the LMK02000 in a typical application. In this setup the clock may be multiplied, reconditioned, and redistributed.



20216570

FIGURE 1. Typical Application

#### 3.2 BIAS PIN

To properly use the device, bypass Bias (pin 36) with a low leakage 1 μF capacitor connected to Vcc. This is important for low noise performance.

#### 3.3 LDO BYPASS

To properly use the device, bypass LDObyp1 (pin 9) with a 10 μF capacitor and LDObyp2 (pin 10) with a 0.1 μF capacitor.



### 3.4 CURRENT CONSUMPTION / POWER DISSIPATION CALCULATIONS

Due to the myriad of possible configurations the following table serves to provide enough information to allow the user to

calculate estimated current consumption of the LMK02000. Unless otherwise noted  $V_{CC} = 3.3\text{ V}$ ,  $T_A = 25\text{ }^\circ\text{C}$ .

**Table 3.4 - Block Current Consumption**

| Block                        | Condition   | Current Consumption at 3.3 V (mA) | Power Dissipated in device (mW) | Power Dissipated in LVPECL emitter resistors (mW) |
|------------------------------|---|-----------------------------------|---------------------------------|---|
| Entire device, core current  | All outputs off; No LVPECL emitter resistors connected                                  | 70                                | 231                             | -   |
| Low clock buffer (internal)  | The low clock buffer is enabled anytime one of CLKout0 through CLKout3 are enabled      | 9                                 | 29.7                            | -   |
| High clock buffer (internal) | The high clock buffer is enabled anytime one of the CLKout4 through CLKout7 are enabled | 9                                 | 29.7                            | -   |
| Output buffers               | LVDS output, bypass mode  | 17.8                              | 58.7                            | -   |
|                              | LVPECL output, bypass mode (includes 120 $\Omega$ emitter resistors)                    | 40                                | 72                              | 60  |
|                              | LVPECL output, disabled mode (includes 120 $\Omega$ emitter resistors)                  | 17.4                              | 38.3                            | 19.1  |
|                              | LVPECL output, disabled mode. No emitter resistors placed; open outputs                 | 0                                 | 0                               | -   |
| Divide circuitry per output  | Divide enabled, divide = 2  | 5.3                               | 17.5                            | -   |
|                              | Divide enabled, divide > 2  | 8.5                               | 28.0                            | -   |
| Delay circuitry per output   | Delay enabled, delay < 8  | 5.8                               | 19.1                            | -   |
|                              | Delay enabled, delay > 7  | 9.9                               | 32.7                            | -   |
| Entire device                | CLKout0 & CLKout4 enabled in bypass mode  | 145.8                             | 421.1                           | 60  |

From Table 3.4 the current consumption can be calculated in any configuration. For example, the current for the entire device with 1 LVDS (CLKout0) & 1 LVPECL (CLKout4) output in bypass mode can be calculated by adding up the following blocks: core current, low clock buffer, high clock buffer, one LVDS output buffer current, and one LVPECL output buffer current. There will also be one LVPECL output drawing emitter current, but some of the power from the current draw is dissipated in the external 120  $\Omega$  resistors which doesn't add to the power dissipation budget for the device. If delays or divides are switched in, then the additional current for these stages needs to be added as well.

For power dissipated by the device, the total current entering the device is multiplied by the voltage at the device minus the power dissipated in any emitter resistors connected to any of the LVPECL outputs. If no emitter resistors are connected to the LVPECL outputs, this power will be 0 watts. For example, in the case of 1 LVDS (CLKout0) & 1 LVPECL (CLKout4) operating at 3.3 volts, we calculate  $3.3\text{ V} \times (70 + 9 + 9 + 17.8 + 40)\text{ mA} = 3.3\text{ V} \times 145.8\text{ mA} = 481.1\text{ mW}$ . Because the LVPECL output (CLKout4) has the emitter resistors hooked up and the power dissipated by these resistors is 60 mW, the total device power dissipation is  $481.1\text{ mW} - 60\text{ mW} = 421.1\text{ mW}$ .

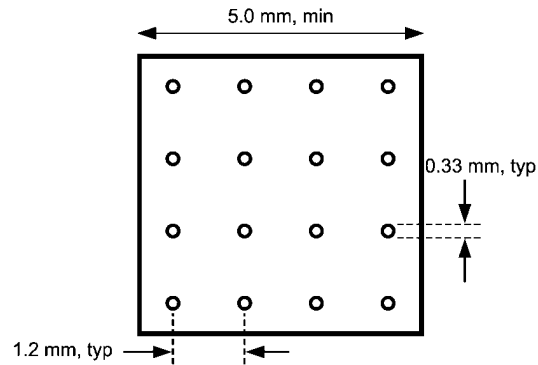
When the LVPECL output is active,  $\sim 1.9\text{ V}$  is the average voltage on each output as calculated from the LVPECL  $V_{oh}$

&  $V_{ol}$  typical specification. Therefore the power dissipated in each emitter resistor is approximately  $(1.9\text{ V})^2 / 120\ \Omega = 30\text{ mW}$ . When the LVPECL output is disabled, the emitter resistor voltage is  $\sim 1.07\text{ V}$ . Therefore the power dissipated in each emitter resistor is approximately  $(1.07\text{ V})^2 / 120\ \Omega = 9.5\text{ mW}$ .

### 3.5 THERMAL MANAGEMENT

Power consumption of the LMK02000 can be high enough to require attention to thermal management. For reliability and performance reasons the die temperature should be limited to a maximum of 125  $^\circ\text{C}$ . That is, as an estimate,  $T_A$  (ambient temperature) plus device power consumption times  $\theta_{JA}$  should not exceed 125  $^\circ\text{C}$ .

The package of the device has an exposed pad that provides the primary heat removal path as well as excellent electrical grounding to the printed circuit board. To maximize the removal of heat from the package a thermal land pattern including multiple vias to a ground plane must be incorporated on the PCB within the footprint of the package. The exposed pad must be soldered down to ensure adequate heat conduction out of the package. A recommended land and via pattern is shown in *Figure 2*. More information on soldering LLP packages can be obtained at [www.national.com](http://www.national.com).



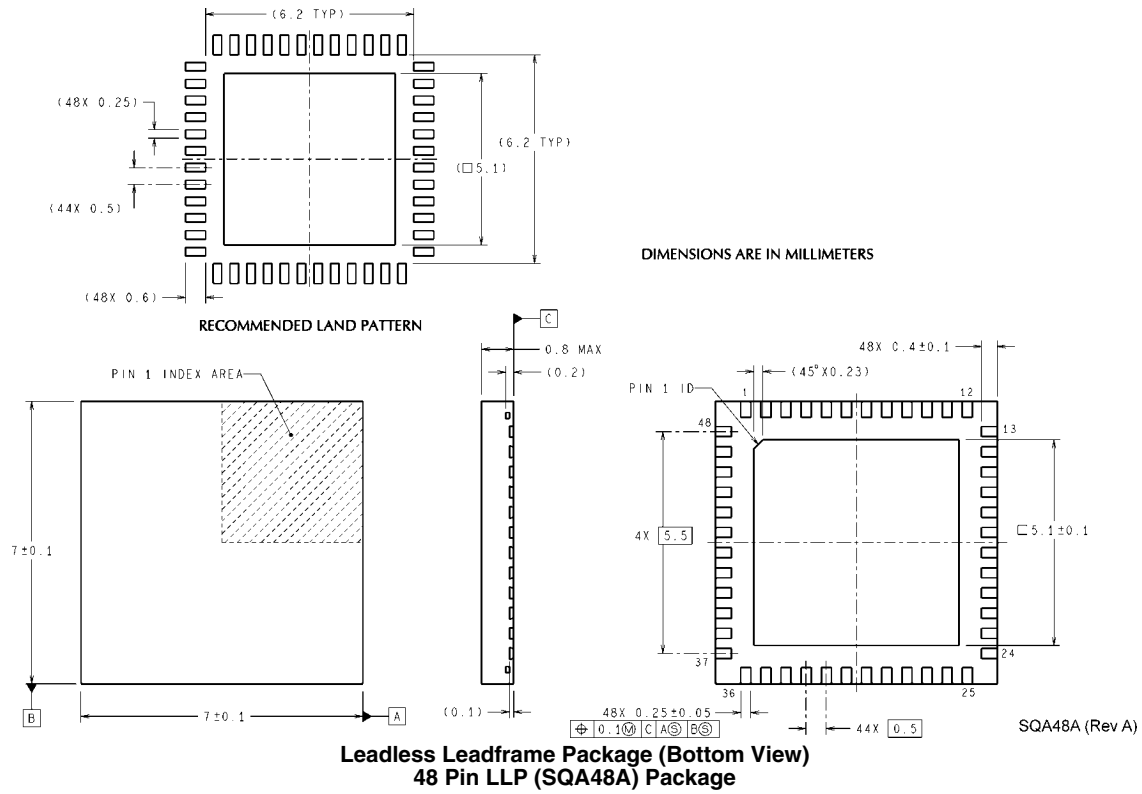
20216573

**FIGURE 2.**

To minimize junction temperature it is recommended that a simple heat sink be built into the PCB (if the ground plane layer is not exposed). This is done by including a copper area of about 2 square inches on the opposite side of the PCB from the device. This copper area may be plated or solder coated to prevent corrosion but should not have conformal coating (if

possible), which could provide thermal insulation. The vias shown in *Figure 2* should connect these top and bottom copper layers and to the ground layer. These vias act as “heat pipes” to carry the thermal energy away from the device side of the board to where it can be more effectively dissipated.

**Physical Dimensions** inches (millimeters) unless otherwise noted



| Order Number | Package Marking | Packing                 | LVDS Outputs | LVPECL Outputs |
|--------------|-----------------|-------------------------|--------------|----------------|
| LMK02000ISQ  | K02000 I        | 250 Unit Tape and Reel  | 3            | 5              |
| LMK02000ISQX | K02000 I        | 2500 Unit Tape and Reel | 3            | 5              |

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